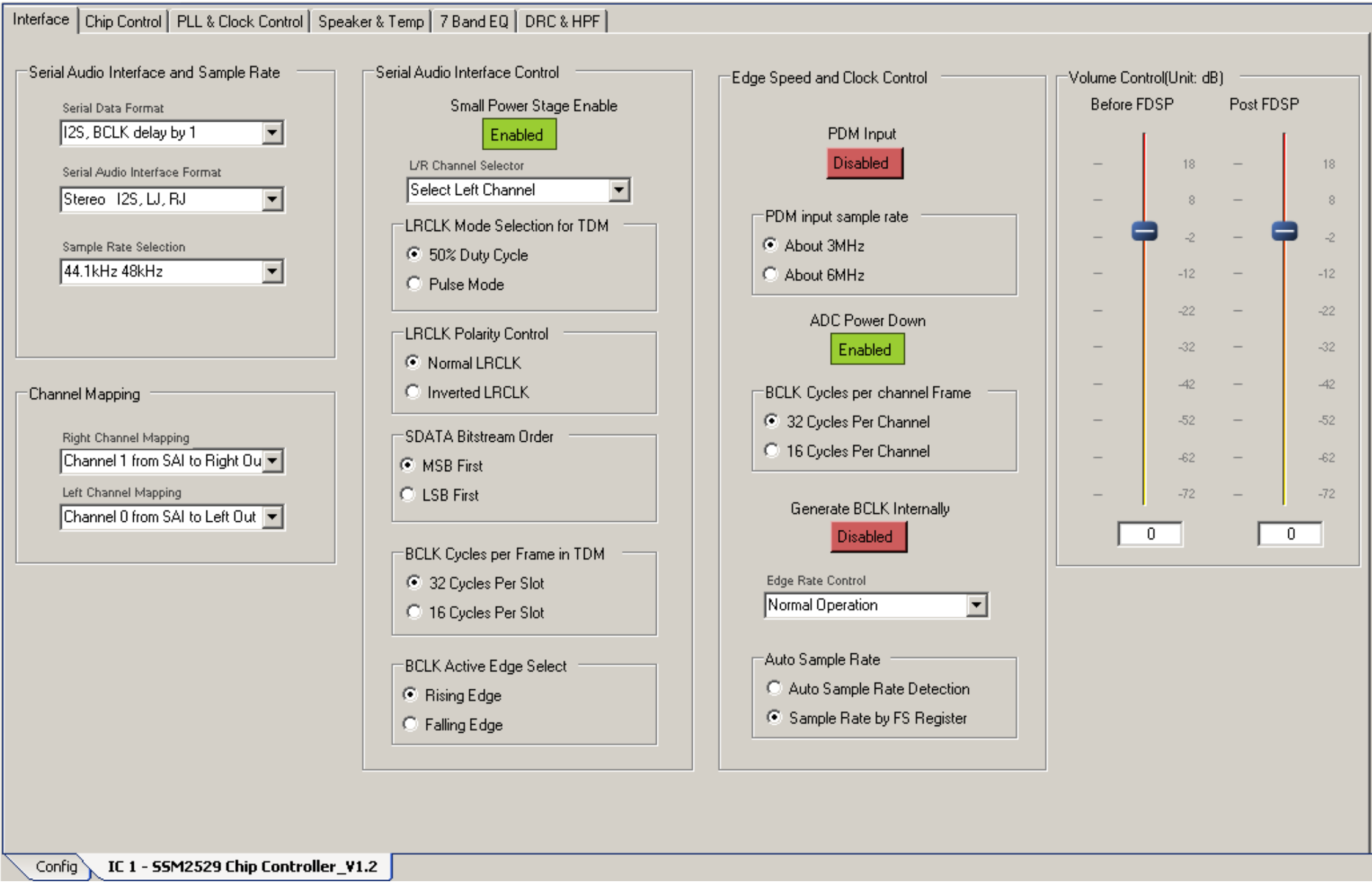
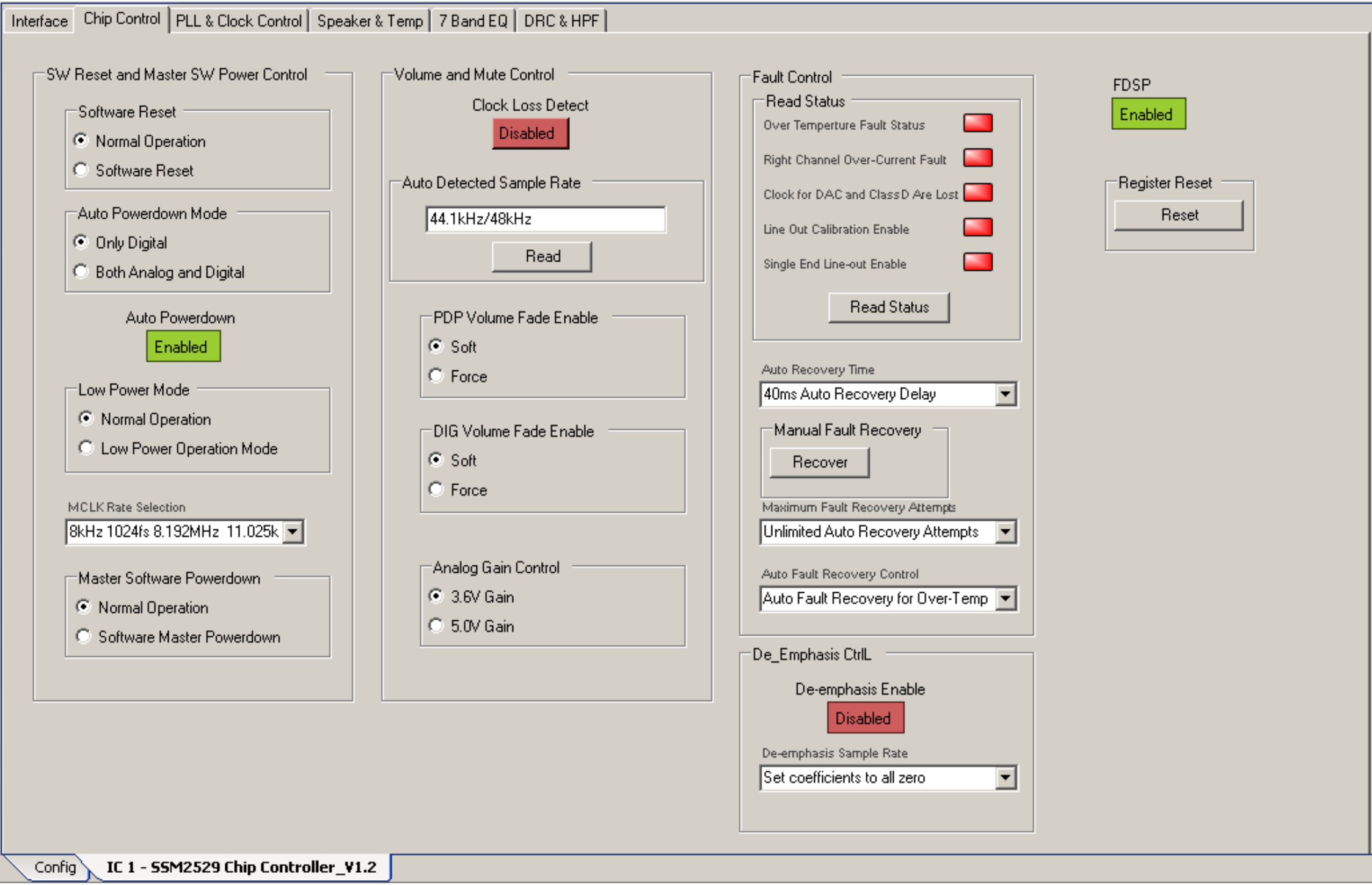
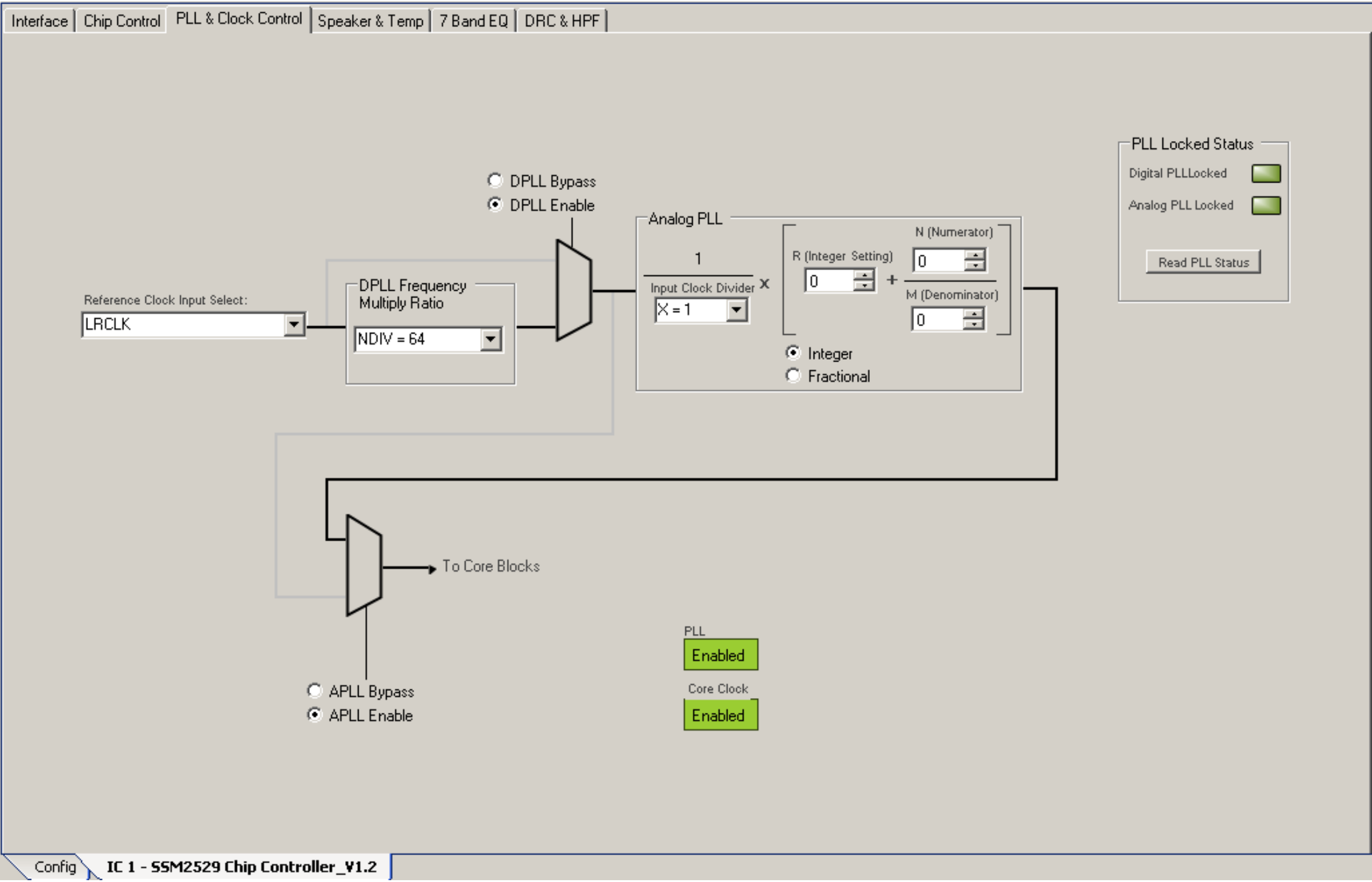
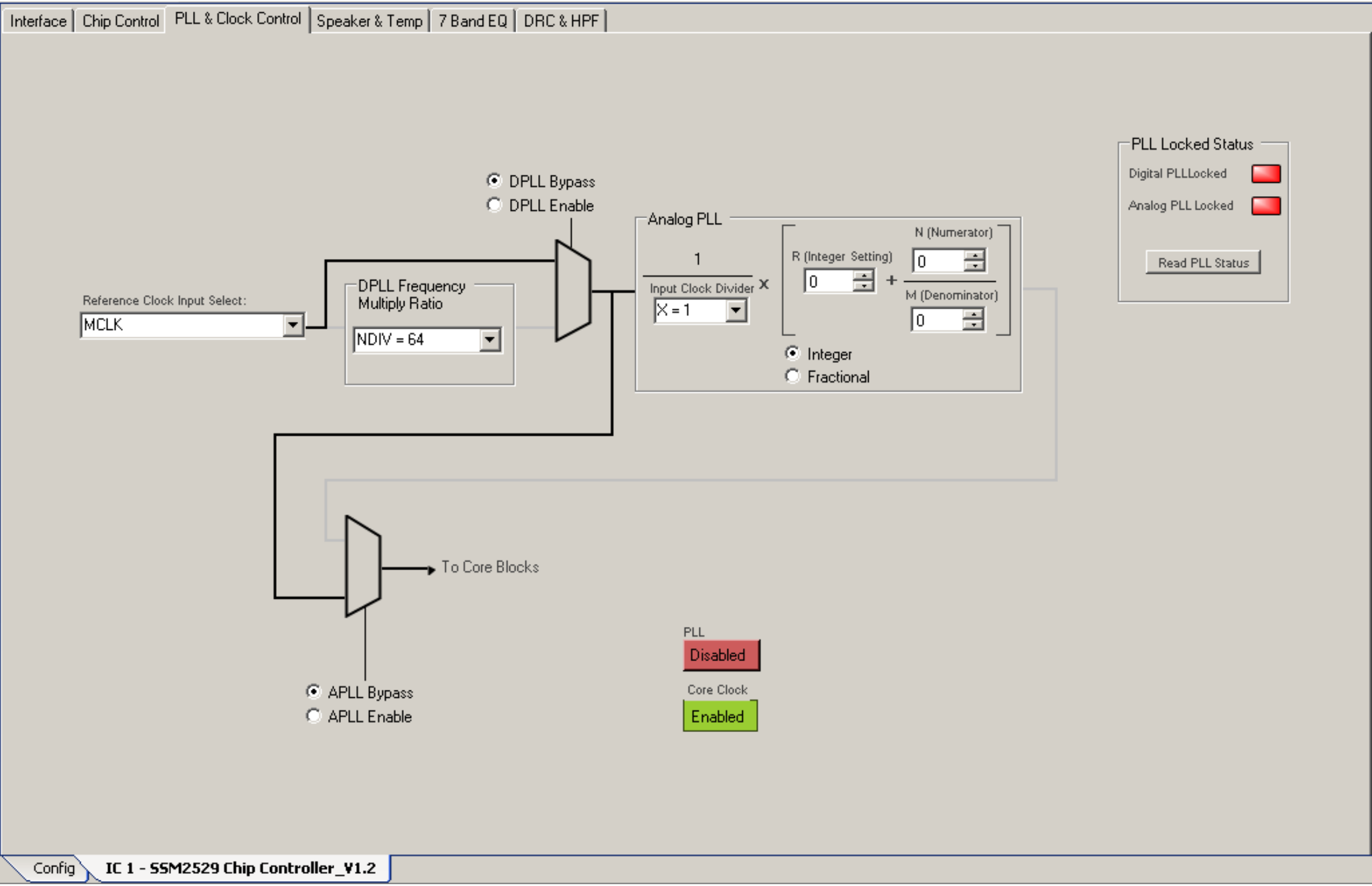

Interface
Chip Control
PLL & Clock Control
Speaker & Temp
7 Band EQ
DRC & HPF
Serial Audio Interface and Sample Rate
Serial Data Format
I2S, BCLK delay by 1
Serial Audio Interface Format
Stereo I2S, LJ, RJ
Sample Rate Selection
44.1kHz 48kHz
Channel Mapping
Right Channel Mapping
Channel 1 from SAI to Right Ou
Left Channel Mapping
Channel 0 from SAI to Left Out
Serial Audio Interface Control
Small Power Stage Enable
Enabled
L/R Channel Selector
Select Left Channel
LRCLK Mode Selection for TDM
50% Duty Cycle
Pulse Mode
LRCLK Polarity Control
Normal LRCLK
Inverted LRCLK
SDATA Bitstream Order
MSB First
LSB First
BCLK Cycles per Frame in TDM
32 Cycles Per Slot
16 Cycles Per Slot
BCLK Active Edge Select
Rising Edge
Falling Edge
Edge Speed and Clock Control
PDM Input
Disabled
PDM input sample rate
About 3MHz
About 6MHz
ADC Power Down
Enabled
BCLK Cycles per channel Frame
32 Cycles Per Channel
16 Cycles Per Channel
Generate BCLK Internally
Disabled
Edge Rate Control
Normal Operation
Auto Sample Rate
Auto Sample Rate Detection
Sample Rate by FS Register
Volume Control(Unit: dB)
Before FDSP
Post FDSP
18
8
-2
-12
-22
-32
-42
-52
-62
-72
0
0
Config
IC 1 - SSM2529 Chip Controller_V1.2


Interface
Chip Control
PLL & Clock Control
Speaker & Temp
7 Band EQ
DRC & HPF
SW Reset and Master SW Power Control
Software Reset
Normal Operation
Software Reset
Auto Powerdown Mode
Only Digital
Both Analog and Digital
Auto Powerdown
Enabled
Low Power Mode
Normal Operation
Low Power Operation Mode
MCLK Rate Selection
8kHz 1024fs 8.192MHz 11.025k
Master Software Powerdown
Normal Operation
Software Master Powerdown
Volume and Mute Control
Clock Loss Detect
Disabled
Auto Detected Sample Rate
44.1kHz/48kHz
Read
PDP Volume Fade Enable
Soft
Force
DIG Volume Fade Enable
Soft
Force
Analog Gain Control
3.6V Gain
5.0V Gain
Fault Control
Read Status
Over Temperture Fault Status
Right Channel Over-Current Fault
Clock for DAC and ClassD Are Lost
Line Out Calibration Enable
Single End Line-out Enable
Read Status
Auto Recovery Time
40ms Auto Recovery Delay
Manual Fault Recovery
Recover
Maximum Fault Recovery Attempts
Unlimited Auto Recovery Attempts
Auto Fault Recovery Control
Auto Fault Recovery for Over-Temp
De_Emphasis CtrlL
De-emphasis Enable
Disabled
De-emphasis Sample Rate
Set coefficients to all zero
FDSP
Enabled
Register Reset
Reset
Config
IC 1 - SSM2529 Chip Controller_V1.2


Interface
Chip Control
PLL & Clock Control
Speaker & Temp
7 Band EQ
DRC & HPF
PLL Locked Status
Digital PLLLocked
Analog PLL Locked
Read PLL Status
DPLL Bypass
DPLL Enable
Analog PLL
1
Input Clock Divider
X = 1
R (Integer Setting)
0
N (Numerator)
0
M (Denominator)
0
Integer
Fractional
Reference Clock Input Select:
LRCLK
DPLL Frequency Multiply Ratio
NDIV = 64
To Core Blocks
APLL Bypass
APLL Enable
PLL
Enabled
Core Clock
Enabled
Config
IC 1 - SSM2529 Chip Controller_V1.2


Interface
Chip Control
PLL & Clock Control
Speaker & Temp
7 Band EQ
DRC & HPF
DPLL Bypass
DPLL Enable
Analog PLL
1
Input Clock Divider
X = 1
x
R (Integer Setting)
0
+
N (Numerator)
0
M (Denominator)
0
Integer
Fractional
PLL Locked Status
Digital PLLLocked
Analog PLL Locked
Read PLL Status
Reference Clock Input Select:
MCLK
DPLL Frequency Multiply Ratio
NDIV = 64
To Core Blocks
APLL Bypass
APLL Enable
PLL
Disabled
Core Clock
Enabled
Config
IC 1 - SSM2529 Chip Controller_V1.2

Interface | Chip Control | PLL & Clock Control | Speaker & Temp | 7 Band EQ | DRC & HPF

## Speaker

Speaker Protection

Disabled

Read Speaker Info

Read

Ambient Temperature

25

Speaker Voice Coil Temperature Status

25

Nominal Speaker DC Resistance

64

Speaker Magnet Temperature Status

25

Nominal Speaker Temperature Coefficient

8

Maximum Speaker Voice Coil Temperature

100

### Speaker Temperature Model

| | |
|---|---|
| Coefficient 1 High: 63 | Coefficient 1 Low: 129 |
| Coefficient 2 High: 0 | Coefficient 2 Low: 85 |
| Coefficient 3 High: 1 | Coefficient 3 Low: 34 |
| Coefficient 4 High: 2 | Coefficient 4 Low: 9 |

## Speaker Protection Gain Control

Attack Rate

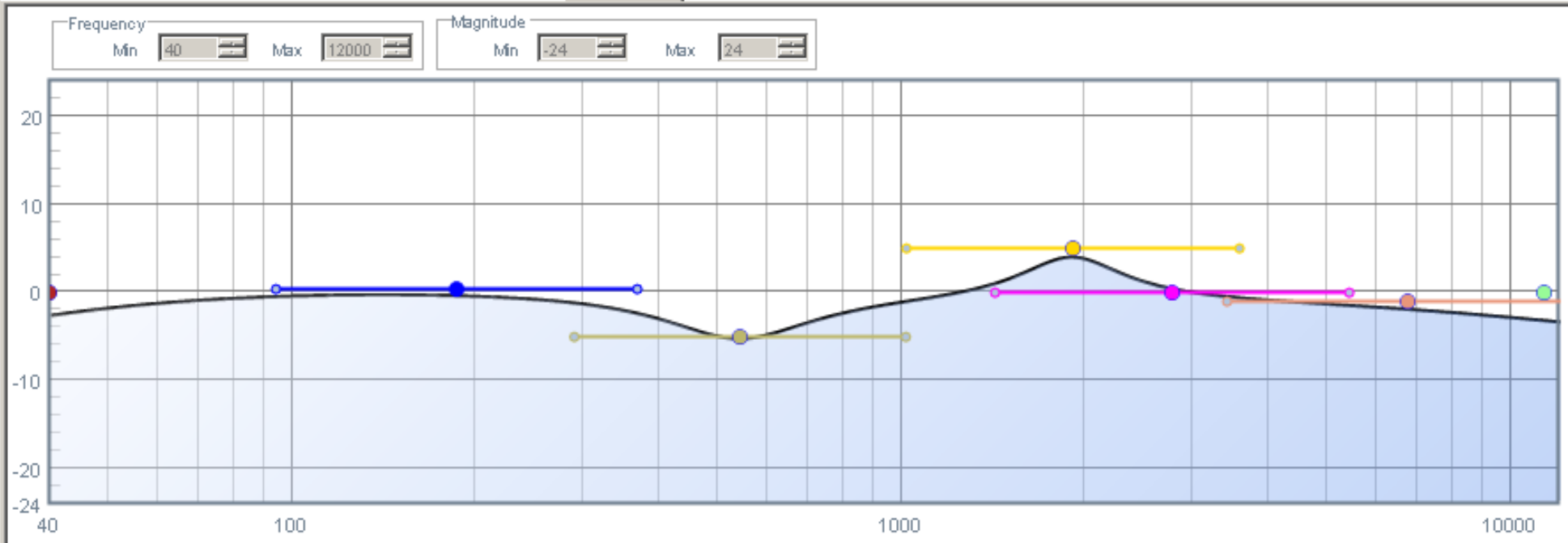
0.009 dB/ms

Release Rate

0.069 dB/s

Config | IC 1 - SSM2529 Chip Controller_V1.2

Interface | Chip Control | PLL & Clock Control | Speaker & Temp | 7 Band EQ | DRC & HPF




| Filter | Frequency1 | Q Factor | Ripple | Boost | Gain1 | Frequency2 | Gain2 | Type | SubType | Active1 | Active2 | View | Bypass | Color |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2783.7 | 0.45 | 0.1 | 0 | 0 | 1000 | 0 | Peaking Filter | 1st Low, 2nd Low | | | | | |
| 2 | 542.5 | 1.41 | 0.1 | -5.04 | 0 | 1000 | 0 | Peaking Filter | 1st Low, 2nd Low | | | | | |
| 3 | 1912.5 | 1.95 | 0.1 | 5.04 | 0 | 30000 | 0 | Peaking Filter | 1st Low, 2nd Low | | | | | |
| 4 | 185.6 | 0.05 | 0.1 | 0.4 | 0 | 1000 | 0 | Peaking Filter | 1st Low, 2nd Low | | | | | |
| 5 | 6788.3 | 0.05 | 0.1 | 0.61 | 0 | 1000 | 0 | Peaking Filter | 1st Low, 2nd Low | | | | | |

**Coefficient Write**

- (•) Automatic EQ Coefficient Update
- ( ) Manual EQ Coefficient Update

EQ Coefficient: Update

**EQ Update Status**

EQ Updating Flag: Read

Clear Update Flag: Clear

**EQ Format**

- (•) 12dB Headroom 13 Bit Precision
- ( ) 18dB Headroom 12 bit Precision

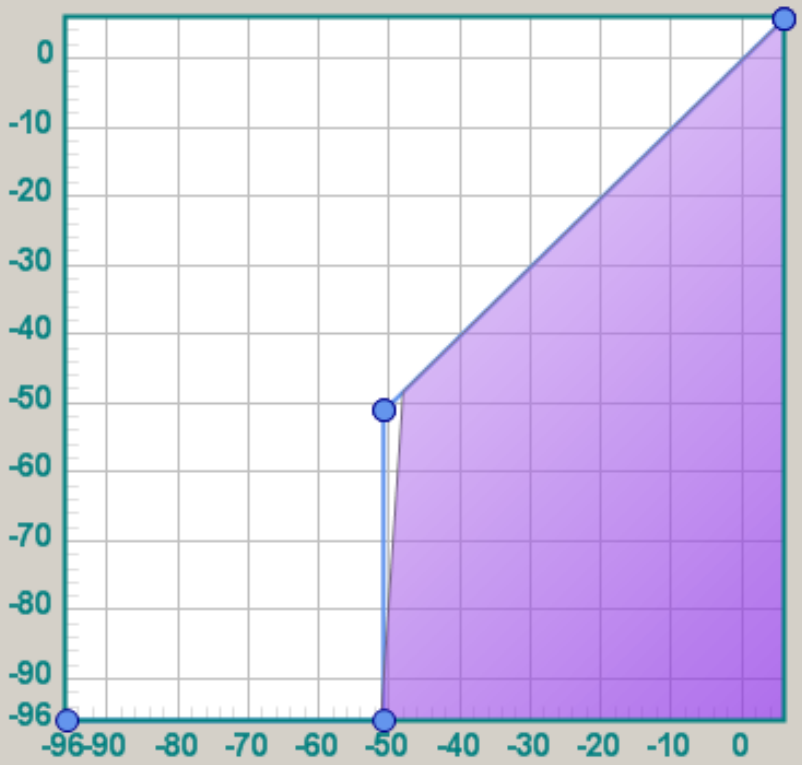
**EQ Enable**

| | | | |
|---|---|---|---|
| Band 1 | Enabled | EQ Overall | Enabled |
| Band 2 | Enabled | | |
| Band 3 | Enabled | | |
| Band 4 | Enabled | | |
| Band 5 | Enabled | | |

Config | IC 1 - SSM2529 Chip Controller_V1.2

Interface | Chip Control | PLL & Clock Control | Speaker & Temp | 7 Band EQ | DRC & HPF

SINGLE BAND DRC




DRC Level Controls(Unit: dB)

| SMIN | Noise Gate | Expander | Compressor | Limiter | SMAX |
|---|---|---|---|---|---|
| -51 | -51 | -51 | 6 | 6 | 6 |

DRC Controls

DRC Enable: DRC Disabled

Ripple Threshold (dB): 0dB (default)

Noise Gate: Enabled

Expander: Enabled

Limiter Source: Peak

Compressor: Enabled

Limiter: Enabled

VBAT tracking: Disabled

DRC Time Constant Controls

| Peak Attack (ms) | Peak Release (ms) | DRC Attack (ms) | DRC Decay (ms) | Noise Gate HoldTime (ms) | Normal Op HoldTime (ms) | RMS Avg Time (ms) |
|---|---|---|---|---|---|---|
| 0 ms | 0 ms | 0 ms | 0 ms | 0 ms | 0 ms | 0 ms |

High Pass Filter

HPF 3dB cut-off frequency: 3.7 Hz (default)

Store/Clear DC Value When HPF Disabled

Clear DC Value

Store DC Value

HPF Enable: Disabled

Config | IC 1 - SSM2529 Chip Controller_V1.2